REMARKS

The claims are claims 1, 3, 4, 6 to 9 and 11.

Claims 1, 3 and 4 were rejected under 35 U.S.C. 103(a) as made obvious by the combination of Wadleigh U.S. Patent No. 6,088,714, Sayegh U.S. Patent No. 5,293,330 and Horton U.S. Patent No. 6,421,696.

Claim 1 recites subject matter not made obvious by the combination of Wadleigh, Sayegh and Horton. Claim 1 recites "disposing said input data into memory, each R continuous data set in continuous memory locations with a space in memory locations from an end of one continuous data set to a beginning of a next continuous data set equal to the size of a cache line." The OFFICE ACTION cites column 13, lines 34 to 63 of Horton as making obvious this limitation. This teaching of Horton differs from the recite limitation in several aspects.

This limitation of claim 1 concerns the memory alignment of the input data. The cited portion of Horton clearly concerns the memory alignment of instructions. The portion of Horton cited in the FINAL REJECTION concerns the code fragment shown in column 13, lines 15 to 20 implementing the initialization of step 410 of Figure 7. The Applicant respectfully submits that it is known in the art that memory data alignment is not the same as memory instruction alignment. This application teaches that instructions are cached in a level 1 program cache 151 separate from the level 1 data cache 157 that stores data. Horton teaches that L1 instruction cache 214 and predocode cache 215 storing instructions are separate from L1 Dcache 226 storing data. Thus the instruction alignment taught Horton fails to make obvious the data alignment recited in claim 1.

Claim 1 recites a differing number of spaces than taught in Horton. Claim 1 recites "each R continuous data set in continuous

memory locations with a space in memory locations from an end of one continuous data set to a beginning of a next continuous data set." This recitation thus requires R-1 such spaces in memory. The teachings of Horton disclose only a single memory alignment corresponding to the dummy instruction "mov eax, eax." Step 410 including this instruction is taught as used for initialization. Thus one skilled in the art would believe that only a single instance of the dummy instruction taught in Horton is required. This single instance cannot make obvious the required plural memory spaces recited in claim 1.

Claim 1 recites a differing amount of memory space than taught in Horton. Claim 1 recites each memory space is "equal to the size of a cache line." Horton does not teach this amount of memory space. Horton states at column 13, lines 36 to 39:

> "This mov instruction serves to displace the starting byte of the subsequent instruction 'lea ebx, [edi*2+edi]' from the end of one cache line to the beginning of the next cache line."

Horton also states at column 17, lines 14 to 17:

> "Instruction (21) is inserted to properly align the subsequent instruction (22), i.e. to displace the starting byte of the subsequent instruction (22) away from an end region of a cache line to the beginning of the succeeding cache line."

These disclosures of Horton teach a differing displacement than recited in claim 1. Claim 1 requires a memory space of an entire cache line. The teaching of Horton states that the displacement moves the next instruction "from the end of one cache line to the beginning of the next cache line" and "away from an end region of a cache line to the beginning of the succeeding cache line." The Applicant respectfully submits that this displacement taught in Horton would ordinarily not result in a memory space "equal to the

size of a cache line" as required by claim 1. The teachings of Horton would result in such a memory space only if the dummy instruction required an entire cache line to store. This is unlikely. Thus the displacement taught in Horton is not the memory space recited in claim 1.

Claim 1 teaches the purpose and effect of the claimed memory space differs from the teaching of Horton. This application teaches at page 29, line 13 to page 33, line 5 that using this memory space for alignment of data in memory avoids many cache conflict misses by assuring that the four input elements of a butterfly map to different cache sets. This application teaches that this mapping to different sets is a consequence of this memory alignment and prevents conflict misses. Horton states at column 13, lines 39 to 53:

> "Instructions such as the load effective address (lea) instruction normally invoke a short decode. However, when the starting byte of such an instruction occurs at the end of a cache line, i.e. in the last one, two, or, in some cases, three bytes of the cache line, predecode unit 212 is unable to determine the length of the instruction to be decoded. Thus, decode unit 220 cannot invoke a fast short decode and must dispatch the instruction to the much slower vector decode unit 256."
>
> "Since it may be especially disadvantageous for the staring byte of a short-decodable instruction to be located at the last one, two, or three bytes of a cache line, instructions may be inserted prior to the short-decodable instruction to displace the short-decodable instruction so as to start in the next succeeding cache line."

This portion of Horton teaches the dummy instruction is inserted to speed decoding of the next instruction. Decoding is speeded by using a short decode when the instruction does not cross a cache line boundary rather than requiring vector decode unit 256 if the instruction crosses a cache line boundary. The Applicant submits that this motivation for aligning instructions taught in Horton so

differs from the motivation to reduce cache misses taught in this application that one skilled in the art would not be motivated to adopt the instruction alignment teaching of Horton to align data as recited in claim 1.

In conclusion, Horton teaches: (1) alignment of instructions rather than alignment of data as recited in claim 1; (2) insertion of a single dummy instruction rather than the plural memory spaces recited in claim 1; (3) insertion of a single instruction to move the following instruction from the end region of one cache line to the beginning of the next cache line rather than the memory space equal to a cache line recited in claim 1; and (4) a different purpose for the alignment, that of speeding instruction decode rather than reducing the number of cache misses as taught in this application. As a consequence of these many differences, Horton fails to make obvious this limitation of claim 1. The FINAL REJECTION does not allege that Wadleigh, Sayegh or their combination teaches this limitation. Accordingly, claim 1 is allowable over the combination of Wadleigh, Sayegh and Horton.

Claims 3 and 4 are allowable by dependent upon allowable claim 1.

The Applicant respectfully requests entry re-consideration of this application. Re-consideration is proper at this time because no changes are proposed to the claims. Thus no new search or reconsideration is required.

The Applicant respectfully submits that all the present claims are allowable for the reasons set forth above. Therefore early entry of this amendment, reconsideration and advance to issue are respectfully requested.

If the Examiner has any questions or other correspondence regarding this application, Applicants request that the Examiner contact Applicants' attorney at the below listed telephone number and address to facilitate prosecution.

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Respectfully submitted,

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